Notice of Allowability	Application No.	Applicant(s)	
	10/803,592	PARK ET AL.	
	Examiner	Art Unit	
	Douglas M. Menz	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/8/06*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *updated search history*.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Hosoon Lee on 7/19/06.

The application has been amended as follows:

Cancel claims 11-20.

Amend claim 5 as follows:

Line 11 of claim 5:

a bit line contact plug layer on the [bit line] contact pad [plug] layer, the bit line contact plug

Drawings

The replacement drawings for figures 8D and 9D were received on 6/8/06. These drawings are acceptable.

Allowable Subject Matter

Claims 1-10 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claims 1-4, there is no teaching or suggestion in the art of record disclosing a semiconductor memory device with a capacitor on a bit line (COB) cell structure comprising a protective layer pattern that covers at least a portion of the second contact pads to prevent the second contact pads from contacting the lower storage node contact plugs, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs and the protective layer pattern, in combination with all other structural limitations of claim 1. Therefore, independent claim 1 is deemed allowable along with its dependent claims 2-4.

Regarding claims 5-10, there is no teaching or suggestion in the art of record disclosing a semiconductor memory device of a COB cell structure in which a plurality of source/drain regions are arranged in a substantially straight line in the length and width directions, comprising a protective layer pattern formed on at least a portion of the second contact pads to prevent the second contact pads from contacting the lower storage node contact plugs, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs and the protective layer pattern, in combination with all other structural limitations of claim 5.

Therefore, independent claim 5 is deemed allowable along with its dependent claims 6-10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M. Menz whose telephone number is 571-272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DM  7/23/06

Updated **EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	587	Hwang.in. and memory and semiconductor	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:01
L2	249	1 and capacitor	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:01
L3	114	2 and (bit adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:01
L4	36	3 and source and drain and contact and plug	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:03
L5	1	4 and ((contact adj pad) and (bit adj line) and substrate and (storage adj node)).clm.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:02
L6	219	257/297.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:08
L13	5	("3970386" | "5346844" | "5389566" | "5451539" | "5631185").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:07
L14	54	("5792687").URPN.	USPAT	OR	ON	2006/07/23 18:07
L15	474	257/298.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:33
L16	715	257/300.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:33
S1	11045	semiconductor and memory and (capacitor with (bit adj line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:12
S2	1228	S1 and substrate and ((source and drain) or source/drain) and pad and dielectric	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:13
S3	457	S2 and contact with plug	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:16

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S4	177	S3 and storage with node	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:17
S5	95	S4 and protect$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:18
S6	0	S5 and interleval adj dielectric	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:18
S7	9	S5 and interlevel adj dielectric	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 13:18
S8	5	("3970386" | "5346844" | "5389566" | "5451539" | "5631185").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/18 13:34
S9	54	("5792687").URPN.	USPAT	OR	ON	2006/07/18 13:35
S10	7	("5389568" | "5405800" | "5543345" | "5554557" | "5923972" | "5926709" | "5956594").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/18 13:42
S11	10	("5065220" | "5143861" | "5352623" | "5597754" | "5726083" | "5744853" | "5792681" | "5804479" | "5879981" | "5895239").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/18 13:43
S12	6	("5407855" | "5510651" | "5665628" | "5668041" | "5854104" | "5990507"). PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/18 13:57
S13	7	("5003428" | "5407855" | "5510651" | "5665628" | "5668041" | "5854104" | "5990507").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/18 13:59
S14	2896	257/296.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:03
S15	2269	Park.in. and memory and semiconductor	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:01
S16	879	S15 and capacitor	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:01

EAST Search History

S17	398	S16 and (bit adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:01
S18	140	S17 and source and drain and contact and plug	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:02
S19	12	S18 and ((contact adj pad) and (bit adj line) and substrate and (storage adj node)).clm.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/23 18:02
S20	1	(capacitor and memory and (isolation adj region) and (contact adj pad) and (bit adj line) and substrate and (storage adj node)).clm.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/18 14:29